REMARKS/ARGUMENTS

In the Office action dated July 1, 2004, claims 1 – 20, 23, 24, 29, 30, 37, 39 – 41, and 48 – 50 were rejected and claims 21, 22, 25 – 28, 31 – 36, 38, and 42 – 47 were objected to. In response, Applicants have canceled claims 2, 11, 32, 42, and 49, amended claims 1, 10, 12, 15, 17, 29, 33, 34, 35, 41, 43, and 48, and added new claims 51 – 57. Applicants hereby request further examination and reconsideration of the application in view of the amended claims, the new claims, and the below-provided remarks.

I. Objections to the Claims

Claims 15, 32, and 35 were objected to because of various informalities. Claim 15 has been amended to delete a redundant occurrence of the phrase "particular one of the plurality of buffers." The limitations of claim 32 have been incorporated into claim 29. The limitations of claim 32 have been amended to recite "read request queues" instead of "write request queues" in line 12 (as originally filed). Claim 35 has been amended to delete the word "an" in line 2.

II. Claim Rejections

Claims 1 – 20, 23, 24, 29, 30, 37, 39 – 41, and 48 – 50 were rejected under 35 U.S.C. 102(e) as being anticipated by Chen et al. (U.S. Patent 6,415,366), hereinafter Chen.

Independent claim 1

Claim 1 has been amended to include the subject matter of claim 2. As amended, claim 1 recites a method to optimally access a memory unit comprising:

> "determining at least one load value of each of the plurality of memory channels;
> based on the determined at least one load value, selecting a particular one of the plurality of memory channels;
> wherein the step of determining the at least one load value of each of the plurality of memory channels includes determining, for each of the plurality of memory channels, the number of pending read requests. (emphasis added)

Claim 1 as filed was rejected in view of Chen. Specifically, the step of "determining at least one load value of each of the plurality of memory channels" was rejected based on column 3, lines 56 – 62 of Chen and the step of "selecting a particular one of the plurality of memory channels" was rejected based on column 2, lines 36 – 39 of Chen. Claim 2 as filed was rejected based on column 2, lines 36 – 39 of Chen.

Chen does not disclose determining the number of pending read requests for each memory channel

Chen discloses a load distribution technique that involves; 1) making an ordered list of memory banks based on the depth of data stored in the banks, where those banks storing the least amount of data are at the top of the list (see col. 4, lines 1 – 12), 2) identifying ineligible banks (e.g., banks that are currently involved in a read or write operation, see col. 4, lines 14 – 19), and 3) selecting the first eligible bank from the ordered list as the bank that will receive the next packet or cell (see col. 4, lines 31 – 38). Although Chen discloses in detail how memory banks are ordered based on bank depth and how memory banks are determined to be ineligible while they are used for other

dequeuing or queuing operations, Chen does not disclose "determining, for each of the plurality of memory channels, the number of pending read requests".

Specifically, with regard to "determining, for each of the plurality of memory channels, the number of pending read requests," Chen discloses that the bank balancer (**100**) "receives dequeue and enqueue information." (Abstract) However, nowhere does Chen disclose that the dequeue and enqueue information includes the number of read or write requests for each memory bank. Further, nowhere does Chen disclose any elements, such as counters, that are used for counting the number of read or write requests for each memory bank. Chen does disclose a "bank depth counter" (see column 3, lines 50 – 62) for counting the depth of data that is stored in each bank but Chen does not disclose any other counters for counting pending read or write requests.

As is well known, a claim is anticipated under 35 U.S.C. 102 only if each and every element as set forth in the claim is found either expressly, or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987) [MPEP 2131] Because Chen does not disclose "determining, for each of the plurality of memory channels, the number of pending read requests" as recited in amended claim 1, Applicants assert that amended claim 1 is not anticipated by Chen.

Claim 3

Claim 3 is dependent on claim 1. Claim 3 recites:

> wherein the step of selecting the particular one of the plurality of memory channels includes selecting the particular one of the plurality of memory channels that has a lowest number of pending read requests." (emphasis added)

Claim 3 as filed was rejected based on column 2, lines 36 – 39 of Chen.

Chen does not disclose selecting a memory channel that has a lowest number of pending read requests

As stated above, although Chen discloses in detail how memory banks are ordered based on bank depth and how memory banks are determined to be ineligible while they

are used for other dequeuing or queuing operations, Chen does not disclose "selecting the particular one of the plurality of memory channels that has a lowest number of pending read requests". Chen discloses that "the bank balancer selects the bank storing the least amount of data that is eligible" (column 2, lines 26 – 27). That is, Chen discloses a bank selection technique that selects whichever bank has the least amount of data stored as long as the bank is eligible (i.e., is not currently involved in a read or write operation). Nowhere does Chen disclose selecting a memory bank that has the lowest number of pending read requests. Because Chen does not disclose "selecting the particular one of the plurality of memory channels that has a lowest number of pending read requests" as recited in claim 3, Applicants assert that claim 3 is not anticipated by Chen.

Claims 4 – 9

Claims 4 – 9 are dependent on claim 1. Applicants assert that claims 4 – 9 are allowable based on an allowable claim 1.

Independent claim 10

Claim 10 has been amended to further define the "determining" step. The additional limitation of amended claim 10 recites:

> "wherein the step of determining the at least one load value of each of the plurality of memory channels includes determining, for each of the plurality of memory channels, at least one of the number of pending read requests and the number of pending write requests."

Amended claim 10 now includes limitations related to determining the number of pending read or write requests for each memory channel. As described above with reference to amended claim 1, Chen does not disclose determining the number of pending read or write requests for each memory bank. Because Chen does not disclose determining the number of pending read or write requests, Applicants assert that amended claim 10 is not anticipated by Chen.

Claims 12 – 16

Claim 12 is amended to correspond to the claim 10 amendments.

Claims 12 – 16 are dependent on claim 10. Applicants assert that claims 12 – 16 are allowable based on an allowable claim 10.

Independent claim 17

Claim 17 has been amended to remove the phase "at least one of" in the determining step. The claim now recites in part:

> "determining, for each of the plurality of memory channels, the number of pending read requests, the number of pending write requests, and the number of active buffers which is the number of a particular one of the plurality of buffers that is unavailable and corresponds to the particular one of the plurality of memory channels in each of the plurality of memory lines;"

The limitations of amended claim 17 now include determining the number of pending read requests for each memory channel, determining the number of pending write requests for each memory channel, and determining the number of active buffers for each memory channel. As described above with reference to amended claim 1, Chen does not disclose determining the number of pending read or write requests for each memory bank. Because Chen does not disclose determining the number of pending read or write requests, Applicants assert that amended claim 17 is not anticipated by Chen.

Claims 18 – 28

Claims 18 – 28 are dependent on claim 17. Applicants assert that claims 18 – 28 are allowable based on an allowable claim 17.

Independent claim 29

Claim 29 has been amended to include the limitations of claim 32 as filed. Claim 29 now includes a pending write request counter, a pending read request counter, and an active buffer counter for each of the memory channels. As described above with reference to claim 1, Chen does not disclose pending read request counters or pending

write request counters. Because Chen does not disclose pending read request counters or pending write request counters, amended claim 29 is not anticipated by Chen.

Claim 33

Claim 33 has been amended to correct the dependency in view of canceled claim 32.

Claim 34

Claim 34 has been amended to depend from claim 30 instead of claim 29. This amendment is made to provide antecedent basis for "the plurality of buffers" and "the plurality of memory lines."

Claims 30, 31, and 33 – 40

Claims 30, 31, and 33 – 40 are dependent on claim 29. Applicants assert that claims 30, 31, and 33 – 40 are allowable based on an allowable claim 29.

Independent claim 48

Claim 48 has been amended to include the limitations of claim 49 as filed except that the phrase "at least one of" in the determining step of claim 49 has been removed. The claim now recites in part:

> "determining, for each of the plurality of memory channels, the number of pending read requests, the number of pending write requests, and the number of active buffers which is the number of a particular one of the plurality of buffers that is unavailable and corresponds to the particular one of the plurality of memory channels in each of the plurality of memory lines;"

The limitations of amended claim 48 now include determining the number of pending read requests for each memory channel, determining the number of pending write requests for each memory channel, and determining the number of active buffers for each memory channel. As described above with reference to amended claim 1, Chen does not disclose determining the number of pending read or write requests for each memory bank. Because Chen does not disclose determining the number of pending read or write requests, Applicants assert that amended claim 48 is not anticipated by Chen.

Claim 50

Claim 50 is dependent on claim 48. Applicants assert that claim 50 is allowable based on an allowable claim 50.

III. Allowable Subject Matter

Applicants note with appreciation that claims 21, 22, 25 – 28, 31 – 36, 38, and 42 – 47 are objected to as being dependent upon rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim. Applicants have rewritten the claims and they appear as amended claim 41 and new claims 51 – 57.

Independent claim 41 (claims 41 + 42)

Claim 41 includes the limitations of claim 42. Applicants assert that claim 41 is in allowable condition.

Claims 43 – 47

Claim 43 has been amended to correct the dependency in view of canceled claim 42. Claims 43 – 47 are dependent on claim 41. Claims 43 – 47 are allowable based on an allowable claim 17.

New independent claim 51 (claims 17 + 18 + 19 +21)

Claim 51 includes the limitations of claims 17, 18, 19, and 21. Applicants assert that claim 51 is in allowable condition.

New independent claim 52 (claims 17 + 18 + 19 +22)

Claim 52 includes the limitations of claims 17, 18, 19, and 22. Applicants assert that claim 52 is in allowable condition.

New independent claim 53 (claims 17 + 18 + 19 +25)

Claim 53 includes the limitations of claims 17, 18, 19, and 25. Applicants assert that claim 53 is in allowable condition.

New independent claim 54 (claims 29 + 31)

Claim 54 includes the limitations of claims 29 and 31. Applicants assert that claim 54 is in allowable condition.

New independent claim 55 (claims 29 + 30 + 34)

Claim 55 includes the limitations of claims 29, 30, and 34. Applicants assert that claim 55 is in allowable condition. Note that the limitations of claim 30 are included in claim 55 to provide proper antecedent basis for "the plurality of buffers" and "the plurality of memory lines."

New independent claim 56 (claims 29 + 35)

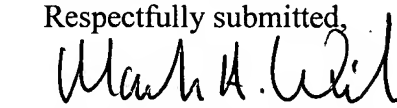
Claim 56 includes the limitations of claims 29 and 35. Applicants assert that claim 56 is in allowable condition.

New independent claim 57 (claims 29 + 30 + 38)

Claim 57 includes the limitations of claims 29, 30, and 38. Applicants assert that claim 57 is in allowable condition.

Applicants respectfully request reconsideration of the claims in view of the remarks made herein. A notice of allowance is earnestly solicited.

Respectfully submitted,



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